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Digital Control of A Multi Level Inverter To Improve Gain And Control Performance

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Abstract: This paper presents The Digital control of Multisampled multilevel inverter(MSMI), As the performance of digital signal processors is an enhancing, applying high sampling frequency becomes increasingly viable, The multisampling technique is developed to minimize the Total Harmonic Distortion(THD), reduce switching delay and increasing the Gain. The filter current ripple frequency is increased by the phase shifted pulse width modulation. The MSMI is contemporized to the peaks of the phase shifted carriers. The small-signal *Z*-domain model is an inferred to examine the MSMI. The MSMI is qualified by the capability of achieving higher feedback control gains, which betters the control performance and reduced the Filter Inductor Ripple Current and THD. The stability boundaries obtained from the root loci showing that the proposed Z-domain models are more effective in forecasting in stabilities, The proposed analysis, and simulation of a MSMI with digital controller closed loop technique 10–kHz switching frequency, 80–kHz sampling frequency Three-phase H-bridge inverter is tested to Five level and Seven levels was verified through MATLAB.

Keywords: Filter Inductor Ripple Current, Multisampled multilevel inverters, Phase-shifted PWM, Small-signal Z-domain model, Digital control system.

I. INTRODUCTION

Presently the digital controllers are increasingly used instead of analog controllers in high power switching converters, since the cost performance ratio of digital signal processors (DSPs) is decreasing [9]. With floating-point DSPs embedding high resolution, high speed analog-to-digital converters (ADCs) and enhanced PWMs, the application of more complicated control algorithms becomes practical. Moreover, although the signals measured from the power circuits contain considerable disturbance around switching instants, sampling algorithms can be used to obtain the average values with reduced switching ripple and noise [1],[2]. Due to these advantages, digital controllers for switching converters have attracted extensive interests during the last decade.

Due to practical limitations of switching devices, the switching frequency cannot be easily increased. However, with the number of the switches increased by multilevel inverters, the filter current ripple frequency can be increased by the phase-shifted PWM strategy [5]. Without changing the switching frequency of each switch, the ripple frequency can be increased in respect to the number of inverter levels [7]. The multisampling is performed according to the number of the phase-shifted carriers.

II. CONTROL STRATEGY

A. Digital Control: In a digital control system, the control algorithm is implemented in a digital computer. The error signal is distinct and fed to the computer by using an A/D (analog to digital) converter. The controller output is again a discrete signal which is applied to the plant after using a D/A (digital to analog) converter. Sampling is a process by which a continuous time signal is converted into a sequence of numbers at discrete time intervals. It is a fundamental property of digital control systems because of the discrete nature of operation of digital computers [9].

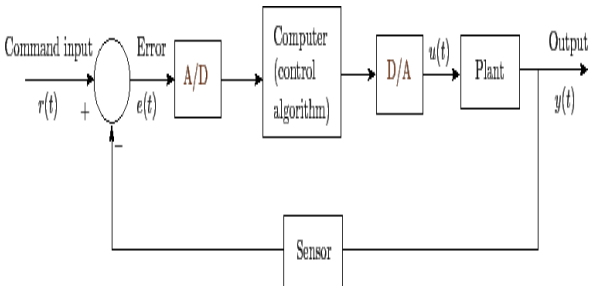

Figure 1.General block diagram of a digital control system

B. Stability Analysis:

The stability of digital control system is based on time domain response and frequency domain response. The time domain response is explained with root locus stability. The frequency domain response is explained with the bode plot [11]. Stability is one of the most important problems of digital control systems, the fundamental stability criterion is zero-pole location adjustment [9]. If a digital control system has all poles inside the unity cycle in z-plane, the system is said to be stable. The stability criterion is demonstrated in the following

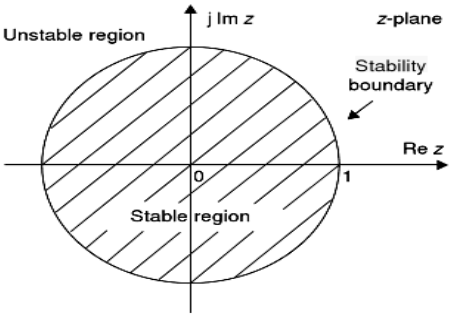

Fig 2. Stable /unstable region in z-plane

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From fig2.the stable region is inside the unity cycle and unstable region is outside the unity-cycle. If pole is located on the cycle it is critically stable [9].

The frequency response method of controller design may be less intuitive than other methods. However, it has certain advantages, especially in real-life situations such as modelling transfer functions from physical data. Frequency response of a system to predict its behaviour in closed-loop. Systems with greater gain margins can withstand greater changes in system parameters before becoming unstable in closed-loop. The phase margin is the difference in phase between the phase curve and -180 degrees at the point corresponding to the frequency that gives us a gain of 0 dB (the gain crossover frequency, W_{gc}). Likewise, the gain margin is the difference between the magnitude curve and 0 dB at the point corresponding to the frequency that gives us a phase of -180 degrees (the phase crossover frequency, W_{pc})[11]

C. Phase Shifted Carriers

This method of carrier signals placement is usually used in H-bridge and FLC converters, but can also be applied in all kinds of multilevel converters. As in other types of sinusoidal modulation, PSC modulation requires n-1 carriers shifted in phase by 360°/n-1, where n is number of levels

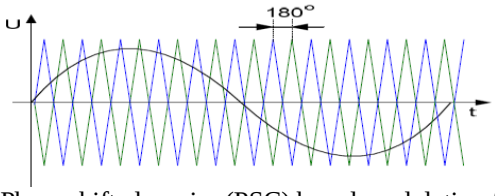

Fig3. Phase shifted carrier (PSC) based modulation for 3 level converter.

Fig.3. presents carrier placement for 3 level converter and one of the commanded voltages. Each carrier is responsible for a pair of switches in all legs of the converter. In three phase system two other phase voltages by comparison with the carriers are generating four more rectangular sequences for the remaining switches[4][6][8]. It is significant in this type of carrier placement that phase to phase voltage reaches three values: 0, 1/3 and 2/3 of DC link voltage in each sampling. In other modulation techniques and carrier signal placement it is possible to avoid non necessary switching of the output voltage,Fig.4. PSC based modulation is widely used in FLC converters because it automatically balances the capacitor voltages [4][8].

III. SMALL SIGNAL Z-DOMAIN ODELLING

The multisampling is performed according to the number of the phase-shifted carriers A classic voltage controller with cascaded control loops for the multilevel inverter, behaving as a typical linear control system. In order to study the improved control performance of the MSMI small-signal z-domain model is derived for the analysis [2][3]. The analysis reveals that higher feedback gains can be employed in the controller of the MSMI, The controller of the stand-alone inverter is a cascaded linear controller composed of an internal current control loop and an external voltage control loop with duty-ratio feed forward (K_{ff} = 1), as is shown in Fig7.

The ideally sampled output voltage and inductor current are represented by[3] v^*_o and i^*_L, respectively. A proportional feedback controller is used in the internal loop with the gain of *kc*, while a proportional plus resonant controller is applied to the external voltage loop[3]. The compensator of the voltage control loop is $G_v(z) = k_v + k_r H_k(z)$, k=1where $Hk(z)$ is the digitalized band-pass filter resonating at kth odd harmonic frequency. The ideally calculated (without delay) digital duty-ratio is x^*, which is updated into the PWM controller with a DSP delay period (analog-to-digital conversion delay and computation delay).The PWM controller updates duty-ratio signal u^*, which is then converted to u_H by a zero-order-hold (ZOH). By comparing u_H to the triangle carrier v_c , the drive signals d and d' are generated.. In order to select the feedback control gains, the model describing the digital control loops is required [3].

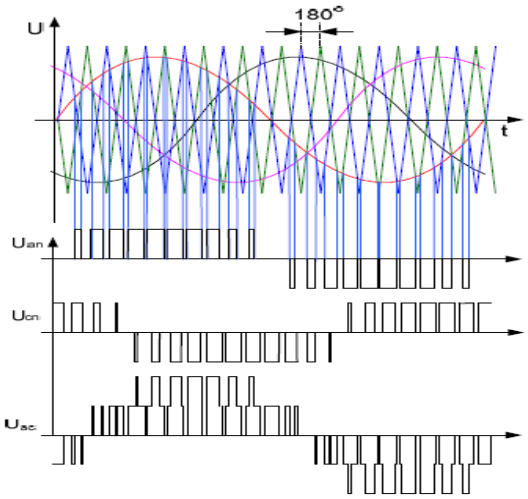

Fig4. Phase and phase to phase voltage generation in PSC based modulation

The key waveform of the bipolar PWM inverter is shown in Fig.7. The carrier is v_c with a switching frequency of $f_s = 1/T_s$. The sampling is synchronized to the time when the PWM counter equals period value. Assuming the total time of analog-to-digital conversion and duty-ratio computation is less than half sampling period, then the calculated duty-ratio can be updated into the compare register at the time when the counter equals zero. Therefore, the DSP delay from x^* to u^* is a half sampling period. As u^* is converted to u_H by a ZOH and the drive signals are generated by comparing u_H with v_c , the PWM delays from u^* to the relevant drive signals in small signal are described by $e^{-s(DTs/2)}$ and $e^{-s(2-D)Ts/2}$, where D is the average duty-ratio scaled in the range of (0,1). Assuming there is no delay from the drive signals to the filter input voltage v_{in}, the small-signal pulse to continuous transfer function describing v_{in} as a function of x^* can be written [3] as

$$Gv_{in}\, x^*(s) = V_{dc}Ts/2(e^{-s\tau d1} + e^{-s\tau d2}) \quad \ldots\ldots\ldots\ldots \quad (1)$$

Where $\tau_{d1} = ((1 + D)Ts/2)$ and $\tau_{d2} = ((3 - D)Ts/2)$.

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When the inverter has no load, the transfer functions describing the inductor current i_L and output voltage v_o as a function of the filter input voltage v_{in} are [3]

$$G_{iL}\ v_{in}\ (s) = \frac{s/L}{s2 + sr_L/L + 1/LC} \quad \text{.....} \qquad (2)$$

$$G_{vo}\ v_{in}\ (s) = \frac{1/LC}{s2 + sr_L/L + 1/LC} \quad \text{.....} \qquad (3)$$

Respectively. Hence, the pulse transfer functions from x^* to the sampled signals i^*_L and v^*_o in small signal are [3]

$$G_{i^*L}\ x^*(z) = Z\{G_{Vin}x^*(s)\ G_{iL}\ v_{in}(s)\} \quad \text{.....} \qquad (4)$$

And

$$G_{v^*o}\ x^*(z) = Z\{G_{Vin}x^*(s)\ G_{vo}\ v_{in}(s)\} \quad \text{.....} \qquad (5)$$

According to Fig. 7, the closed-loop transfer function from i^*_{ref} to x^*without feed forward can be written as [3]

$$G_1(z) = \frac{k_c/V_{d\,c}}{1 + k_c/Vd\ c\ Gi^*L\ x^*(z)} \qquad (6)$$

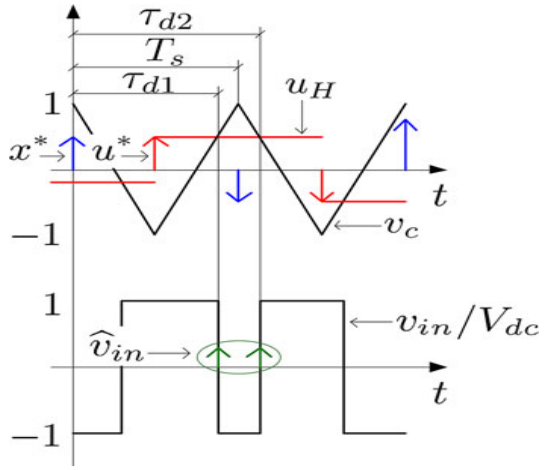

Fig 5. Time domain wave forms of uniform sampling [3]

IV. MULTISAMPLED MULTILEVEL INVERTERS

To demonstrate the improved control performance as a result of the multisampled multilevel inverter, this section provides a detailed analysis of the system's operation in contrast to the bipolar switched inverter.

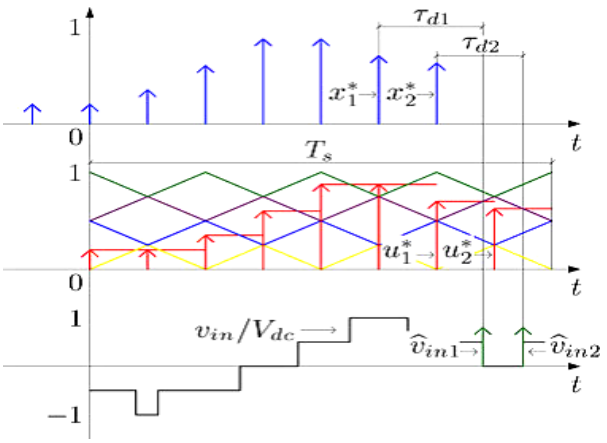

Fig 6. multi sampling time domain wave forms

A system comprised of two cascaded H-bridges inverters and modulated by four phase-shifted triangle carriers with octuple-sampling frequency is modeled. The analysis is undertaken to assess the performance advantages of the multisampled multilevel inverter [3].

The modulation model can be obtained by describing the small-signal filter input voltage v_{in} a function of x^* that when x^* is changing slowly compared to the carriers, the delay effect can be determined by the average duty-ratio D. If the drive signal is generated in the duration of the rising edge of the carriers in equation (1)[3].

The delay effect is expressed as $e-s\tau d\ 1$,
Where $\tau d1 = DTs/2-$ floor $(TsN/2) + Ts/N$
With the multisampling factor $N = 8$.

The delay effect is expressed as $e-s\tau d\ 1$, where $\tau d1 = DTs/2-$floor $(TsN/2) + Ts/N$ with the multisampling factor $N = 8$. On the other hand, when the drive signal is generated during the falling edge of the carriers , the delay effect is written as $e-s\tau d\ 2$, with $\tau d2 = (1-D)Ts/2-$ floor$(N\ (1-D)\ Ts\ /2) + Ts/N$. Since the exact double-update-mode PWM model cannot be obtained straightforwardly, an approximation can be derived by averaging the delay effects and the small-signal transfer Function is written as [3]

$$Gv_{in}\ x^*\ (s) = VdcTs/2N(e-s\tau d\ 1 + e-s\tau d\ 2\ ) \quad \text{.....} \quad (6.1)$$

When the inverter has no load, the transfer functions describing the inductor current iL and output voltage v_o as a function of the filter input voltage v_{in} are [3]

$$G_{vo\ Vin}\ (s) = \frac{\frac{1}{LC}}{s^2+s\frac{rl}{LC}+\frac{1}{LC}} \quad \text{.....} \qquad (7)$$

$$G_{iLvin}(s) = \frac{\frac{s}{L}}{s^2+s\frac{rl}{LC}+\frac{1}{LC}} \quad \text{.....} \qquad (8)$$

Respectively. Hence, the pulse transfer functions from x^* to the sampled signals i^*L and v^*o in small signal are [10]

$$G_{i_L^*\,x^*}(z) = \mathcal{Z}\{G_{v_{in}\,x^*}(s)G_{i_L\,v_{in}}(s)\} \quad \text{.....} \qquad (9)$$

And

$$G_{v_o^*\,x^*}(z) = \mathcal{Z}\{G_{v_{in}\,x^*}(s)G_{v_o\,v_{in}}(s)\} \quad \text{.....} \qquad (10)$$

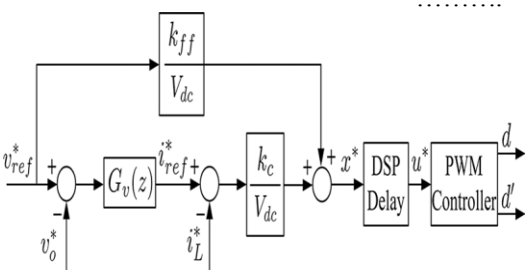

Fig7. Digital controller of cascaded multi level inverter

V. SIMULATION RESULTS

In This paper the system consists of CMLI single phase uniformly sampled, multisampled 3phase multilevel inverter and LC filter and dc source are used. For the generation of pulses, the digital controller system used. The dc supply into ac supply by using cascaded multi level inverter with digital controller of uniformly sampled multi

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sampled multi level inverter was done. In this paper normal inverter is replaced with an CMLI single phase and three phase multilevel inverter to reduce harmonics in the supply with the digital control technique In this paper Digital controlled multi level inverter with LC filter is used to eliminate total harmonics present in the supply.

A. *Simulation results of uniformly sampled bipolar switched inverter is shown*

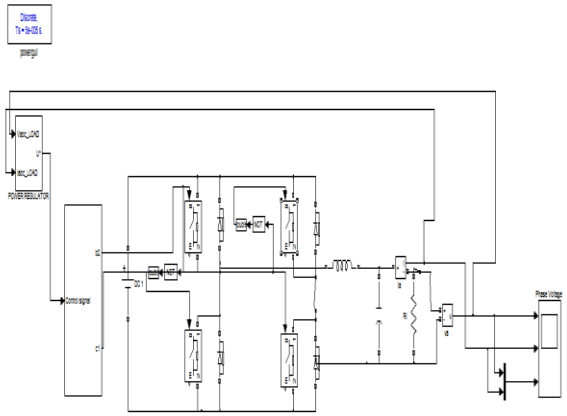

Fig7. Simulation diagram of uniformly sampled bipolar switched inverter

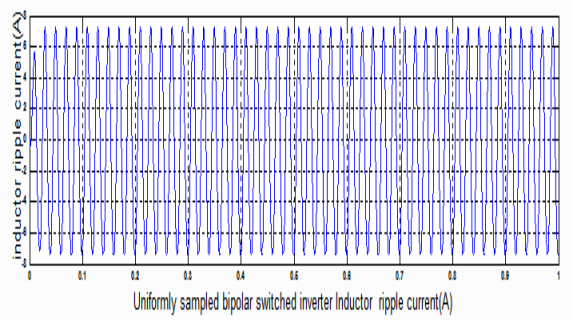

Fig7 (a).uniformly sampled bipolar switched inverter ripple currents(A)

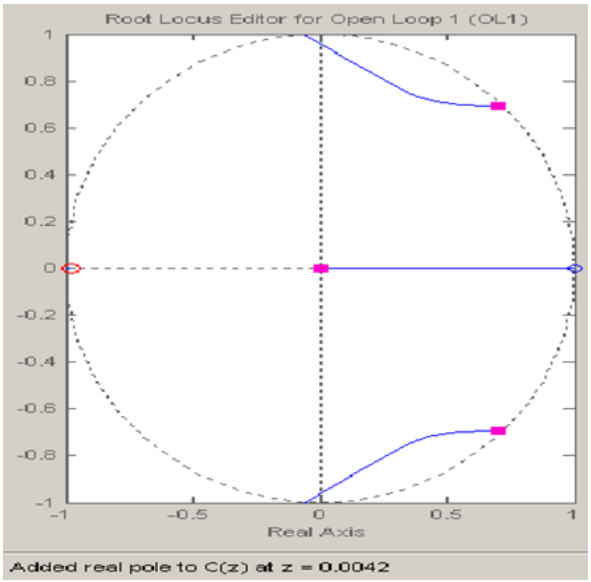

Fig7 (b).Root locus analysis of uniformly sampled bipolar switched inverter for Current loop

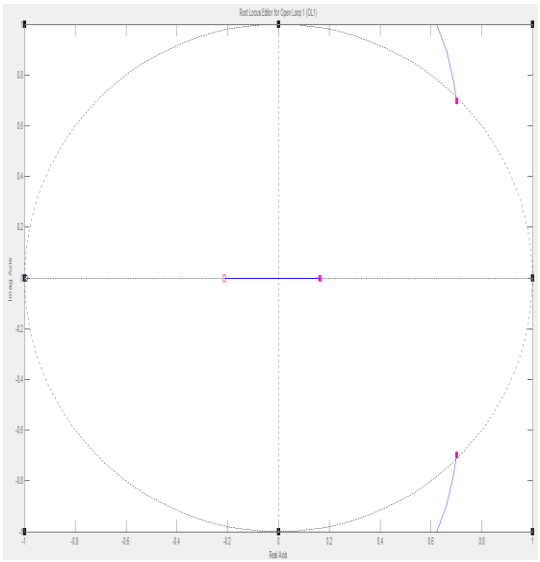

Fig7(c).Root locus analysis of uniformly sampled bipolar switched inverter for Voltage Loop

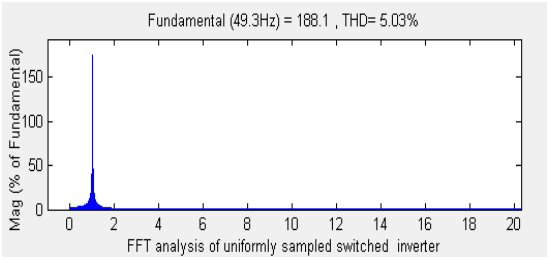

Fig7(d).Total harmonic distortion uniformly sampled bipolar switched inverter

B. Simulation results of multisampled 5level inverter

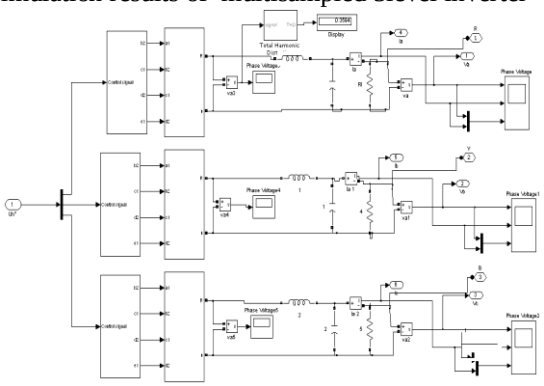

Fig8. Simulation diagram of five level inverter

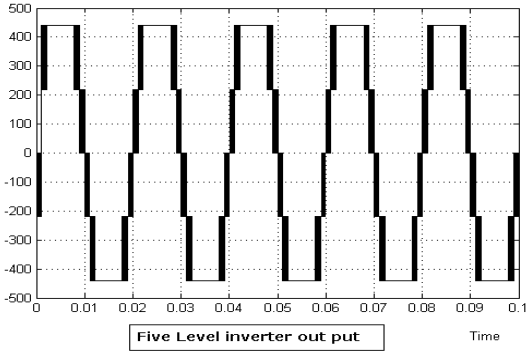

Fig8(a). 5 Level Inverter output Voltage

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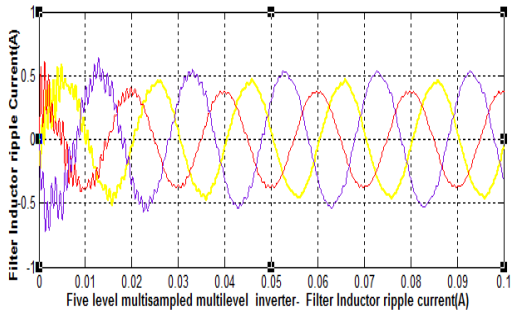

Fig8(b). Filter Inductor ripple current (A) of five level inverter waveform

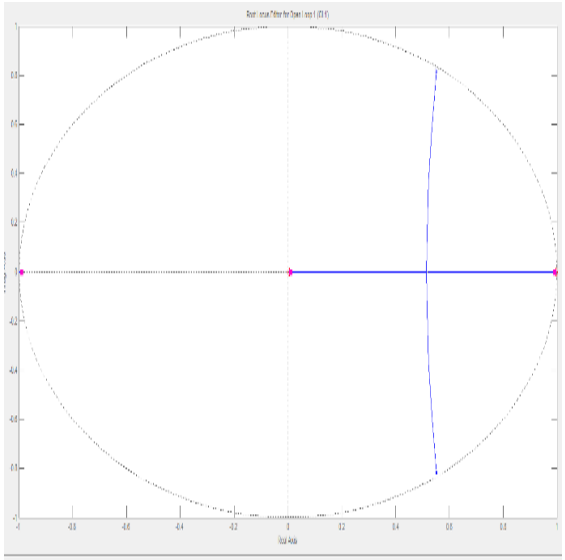

Fig8(c). Root locus analysis of multi sampled five level inverter for Current loop

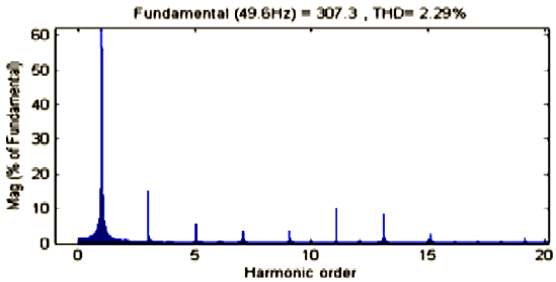

Fig8(f). Total harmonic distortion analysis of 5 level multisampled inverter with non-linear load

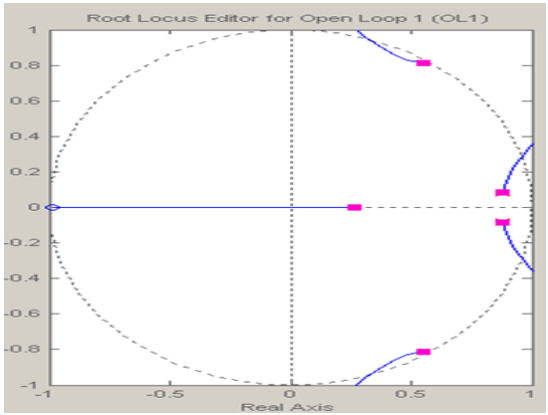

Fig8(d). Root locus analysis of multi sampled five level for Voltage Loop

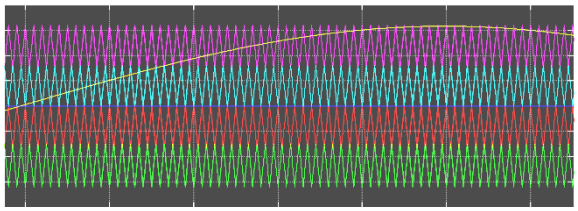

Fig8(e). The phase shifted PWM 5 level inverter.

C. Simulation results of multisampled 7level inverter

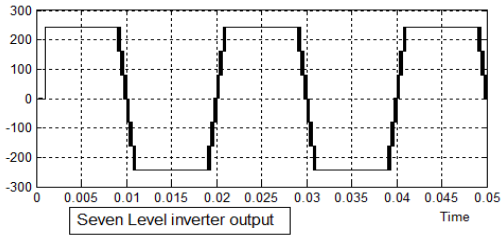

Fig9.7 level inverter output voltage waveforms

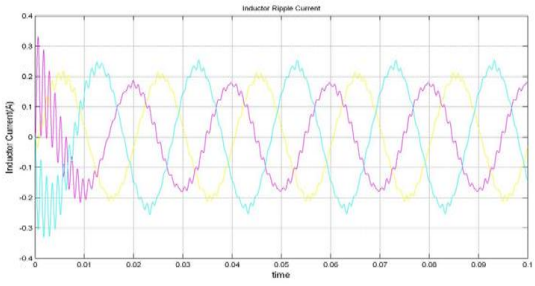

Fig9(a).Filter inductor ripple current(A) of 7level inverter waveform

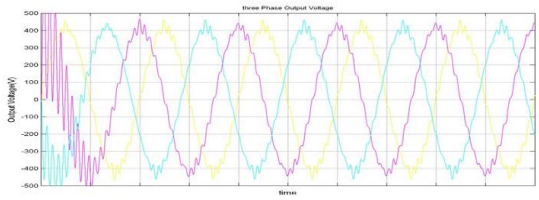

Fig9(b).seven level inverter output voltages

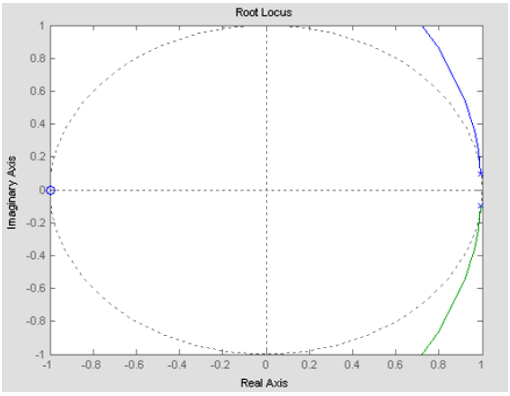

Fig9(c). Root locus analysis of seven level inverter

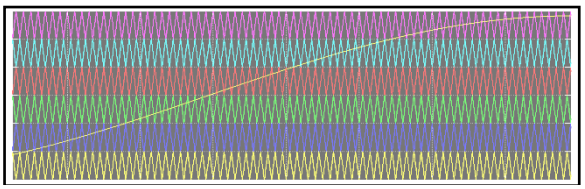

Fig9(d). The phase shifted PWM 7 level inverter

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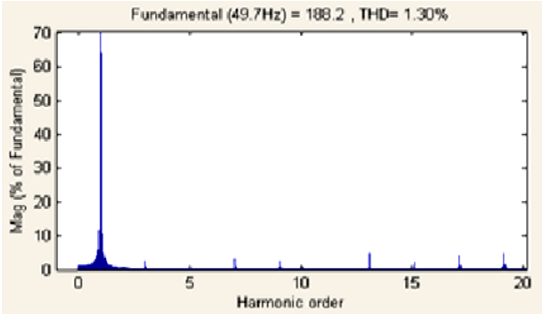

Fig9(e). Total harmonic distortion analysis of 7level inverter output voltage

Table1. Comparison of THD result analysis for uniform sampling and multi sampling

Uniform sampling	Multi sampled **five** level inverter	Multi sampled **seven** level inverter
5.03%	2.29%	1.30%

Table 2. Comparison of Filter Inductor Ripple Currents

Uniformly sampled bipolar switched inverter **Inductor ripple current** (peak to peak)	**Multi sampled Five** level **Inductor ripple current** (peak to peak)	**Multi sampled Seven** level **Inductor ripple current** (peak to peak)
7.5A	**1A**	**0.5A**

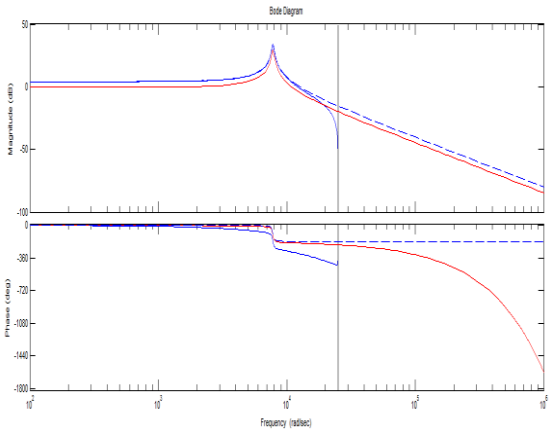

Fig9 (f). Comparison of bode plot analysis

Uniformly sampled bipolar switched inverter (Blue-colour)
Seven level inverter (continues Line-Blue)
Five level inverter (Red-colour)

Table3. Comparison of Gain analysis of Uniform sampling and Multi sampling

Uniformly sampled bipolar switched inverter	**Multi sampled Five** level inverter	**Multi sampled Seven** level inverter
0.8	0.98	1.2

Table4. Load parameters of Seven Level Inverter

Quantity	**Value**
DC voltage Amplitude	250
Switching period	100µs
Sampling period	0.0000125s
Inductor	1642µH
Capacitor	10µF
Inductor parasite resistance	0.4 Ω

In this paper the comparison of uniformly sampled bipolar inverter, phase shifted five levels and seven level inverter and their time domain and frequency domain analysis was done. The THD analysis was compared. The bode and root locus plots were used to explain the stability analysis and control gains to improve control performance. The table1. Shows the THD comparisons of uniformly sampled and multi sampled multi level inverters. From the table 2.explite the Comparison of Filter Inductor Ripple Currents, From the table 3. Comparison of Gain analysis of Uniform sampling and Multisampling methods. The table 4, Shows the parameters Value in the simulation work done. In this paper the Digital control of a multisampled multilevel inverter, improved the Gain and control performance are An Exploited that from Table1, Table2, and Table3.

VI. CONCLUSION

This paper proposed the digital control method is to overcome the problem of high ripple current and reduction of total harmonic distortion more over the output voltage reaches a steady state within few cycles, which improves the control performance. The results obtained from a Five Level and seven-level inverters With R load, Non-linear loads are examined and compared with bipolar switched inverter MATLAB/SIMULINK used to validate the analysis.

1) The feasibility of employing higher gains to achieve better control performance in the multisampled multilevel inverter. The uniformly sampled inverter gain was 0.8 and multi sampled multi (five and seven) level inverter has gains as 0.9 and 1.2 stability was increased.

2) The harmonic content was reduced. Uniform sampling inverter has THD as 5.03%,Multi sampled five level inverter has THD as 2.29% and seven level inverter has THD as 1.30%. **3)** By using the phase-shifted PWM method in multilevel inverters, the filter current ripple frequency is increased, the uniformly sampled inverter operate equal sampling and switching frequency, where as five level inverter can operate octuple frequency which allows the controller to achieve better performance. We can conclude that the multisampled multi level inverter is designed to reduce the harmonics present in the system, by using digital controller technique. And the control gains are increased to achieve better performance.

VII. FUTURE SCOPE

By using Multi sampled multilevel inverter with an LC filter, THD analysis of output current waveform is

reduced, the system gains are increased to get the system stability. The THD can be reduced more by modifying this circuit further more like replacing higher number of levels inverter using digital control technique and others

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